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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,364	06/26/2003	Kyoung-Moon Lim	0630-1717P	4532

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EXAMINER	
SHANKAR, VIJAY	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	02/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 02/09/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/606,364	LIM, KYOUNG-MOON	
	Examiner	Art Unit	
	VIJAY SHANKAR	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-15 and 18* is/are allowed.

6)☒ Claim(s) *1-4,16,17 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4,16-17, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al (6,331,844 B1) in view of Hush et al (6,069,451).

Regarding Claim 1, Okumura et al teaches a driving circuit for a flat panel display , the circuit comprising: a latch unit (Figs.1-3; Column 7, lines 15-50) to which a control signal is applied from a shift register (Figs.1-3; Column 7, lines 15-50) to sample at least one digital picture signal and to store the digital picture signal (see Col.11, lines 23-60), and the latch unit simultaneously outputting the sampled picture signals by a line pass signal (Figs.1-3; Column 7, lines 15-50; Col.11, lines 23-60); and a voltage to current converting unit (Fig.2; Column 9, lines 35-Col.10, line 67) supplying current of a plurality of levels to a data line of the display panel according to logical

combinations of the sampled picture signal from the latch unit, using a current mirror method (Figure 5; Col.11, lines 59-Col.12, line 29). Also, see Figs.1-5; Column 7, lines 15-50; Column 9, lines 35-Col.10, line 67; Col.11, line 23-67). However, Okumura doe not teach that a voltage to current converting unit comprises a current mirror circuit and wherein the voltage to current converting unit includes switching units formed on the display panel.

Hush et al teaches a voltage to current converting unit comprises a current mirror circuit (see Col.3, lines 60- 67; Col.6, lines 15-17) and wherein the voltage to current converting unit includes switching units formed on the display panel (Summary; Fig.1; Col. 2, line 61- Col.2, line 67).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the teaching of Hush et al into Okumura et al for reducing the cost of the display.

Regarding Claim 2, Okumura et al teaches a circuit wherein the latch unit comprises: a first latch unit being applied the control signal from the shift register to sample and store a digital picture signal having a plurality of bit numbers (Figs.1-3; Column 7, lines 15-50; Col.11, lines 23-60) ; and a second latch unit outputting the digital picture signal sampled in the first latch unit simultaneously according to an outer line-pass signal. (Figs.1-3; Column 7, lines 15-50; Col.11, lines 23-60).

Regarding Claims 3-4, 21, Okumura et al teaches a circuit wherein the shift register, the latch unit and the voltage to current converting unit are formed in the display panel. (Figs.1-3; Column 7, lines 15-50), and the display panel is an organic electroluminescence display panel. (Background, summary).

Regarding Claims 16-17, Okumura et al teaches the circuit wherein the voltage to current converting unit includes a current mirror with plurality of current paths. (Figure 5; Col.11, lines 59-Col.12, line 29).

Regarding Claim 19, Okumura et al teaches the flat panel display, comprising: a substrate; a plurality of pixel units located on the substrate; and a data driving circuit located on the same substrate, the data driving circuit including a plurality of current paths, the data driving circuit supplying current of a plurality of levels to at least one of the plurality of pixel units by providing the current from at least one of the plurality of current paths. (Figure 5; Col.11, lines 59-Col.12, line 29). Also, see Figs.1-5; Column 7, lines 15-50; Column 9, lines 35-Col.10, line 67; Col.11, line 23-67). However, Okumura doe not teach the current mirror paths are formed on the substrate.

Hush et al teaches the current mirror paths are formed on the substrate (Summary; Fig.1; Col. 2, line 61- Col.2, line 67; Col.3, lines 60- 67; Col.6, lines 15-17).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the teaching of Hush et al into Okumura et al for reducing the cost of the display.

Regarding Claim 20, Okumura et al teaches the flat panel display wherein the data driving circuit includes a current mirror structure on the same substrate, the current mirror structure receiving a reference current to provide the current from the at least one of the plurality of current paths based upon logical combinations of bits of a digital picture signal. (Figure 5; Col.11, lines 23-Col.12, line 29).

Allowable Subject Matter

3. Claims 5-15 and 18 are allowed.

2. The following is an examiner's statement of reasons for allowance: The prior arts fail to teach a driving circuit for a flat panel display wherein the voltage to current converting unit comprises: **a first switching unit for controlling a flow of a reference current by an enable signal; a second switching unit connected to the first switching unit for controlling the flow of the reference signal by the enable signal; a first NMOS transistor for forming a reference path on which the reference current flows between the first switching unit and ground by being applied the reference current on a gate electrode thereof; a plurality of NMOS transistors not**

including the first NMOS transistor for forming a plurality of current paths in a parallel direction between the data line and the ground of the display panel according to picture signals having a plurality of bit numbers by being applied the reference signal on respective gate electrodes thereof; and a plurality of switching units for controlling switching of the plurality of current paths by being applied the picture signal having the plurality of bit numbers independently as claimed in Claim 5 and 18.

Also, Claims 6-15 are allowable because it depends on Claim 5 and 18.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

3. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIJAY SHANKAR whose telephone number is (571) 272-7682. The examiner can normally be reached on M-F 7:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIJAY SHANKAR
Primary Examiner
Art Unit 2673

VS